Reconfigurable Architecture (1)

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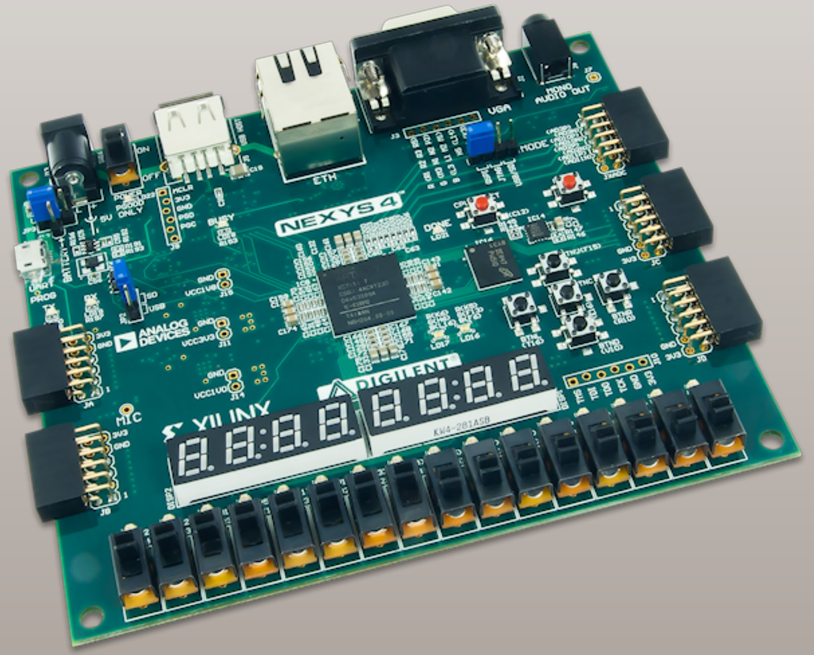
- Interruptions are welcome: ask me anything in the class
  - Off-class discussion on Slack is also welcome
  - We may have separate class in English, but single class will be better…?

Overview

- FPGAs and other reconfigurable devices
  - Organization of the devices
  - Design methodology: HDL, HLS and embedded software
- Lecture and hands-on
  - Xilinx Vivado + Digilent Nexys4 (Artix-7 100T)

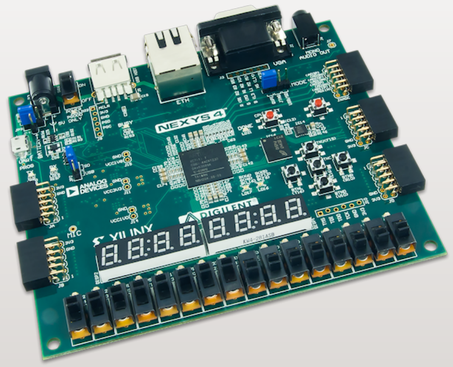


For your research

- Get a job in LSI design world ?
- Custom hardware for your own research
  - For timing-accurate or high-speed control, compared to MCUs
  - Fast / real-time control and signal processing

Goal of this class

- Understand the device organization
- Be familiar with the design tools
  - Apply in your own research
  - What do you want to solve with FPGAs?



Artix-7 XC7A100T

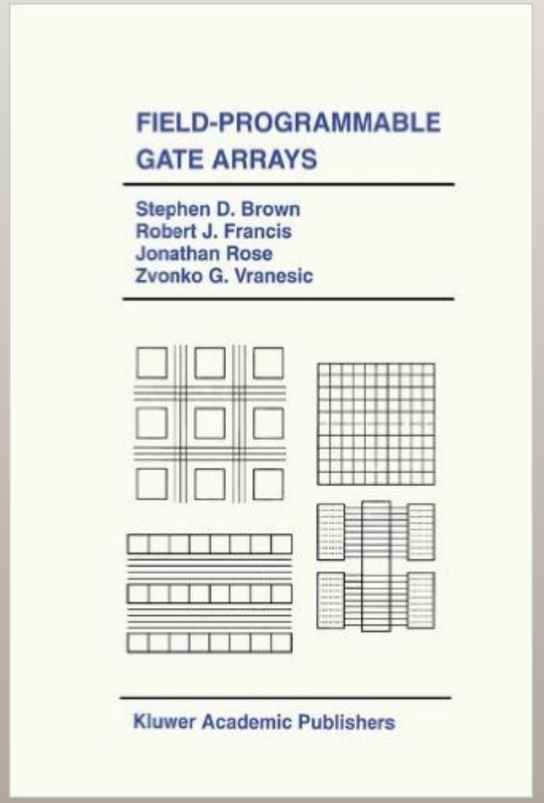
Kintex-7 XC7K325T

Lecture and Hands-on

- Lecture:
  - Device architecture, CAD algorithm and Design method
  - Real-world application examples
- Hands-on: HDL (Verilog)、CAD (Vivado HLx + SDK)
  - with reports / assignments

Textbooks

* Get your copy only if you're **really** interested in…
  * English/Chinese translations are published



Lecture materials & Slack channel

* Should be available with other coarse materials (but not ready for 2020 yet)
  * http://mux.eee.u-ryukyu.ac.jp/lecture.html.en (or .html.ja for older versions)
* Invited all students for slack workspace: please join
* You can record this class, but please do not disclose to everyone

LSI: Large-Scale Integrated circuit

- Very small transistors and wires on silicon substrate
- Analog and Digital circuits on a chip
  - Variety from OP amps to microprocessors

Good old days of LSIs

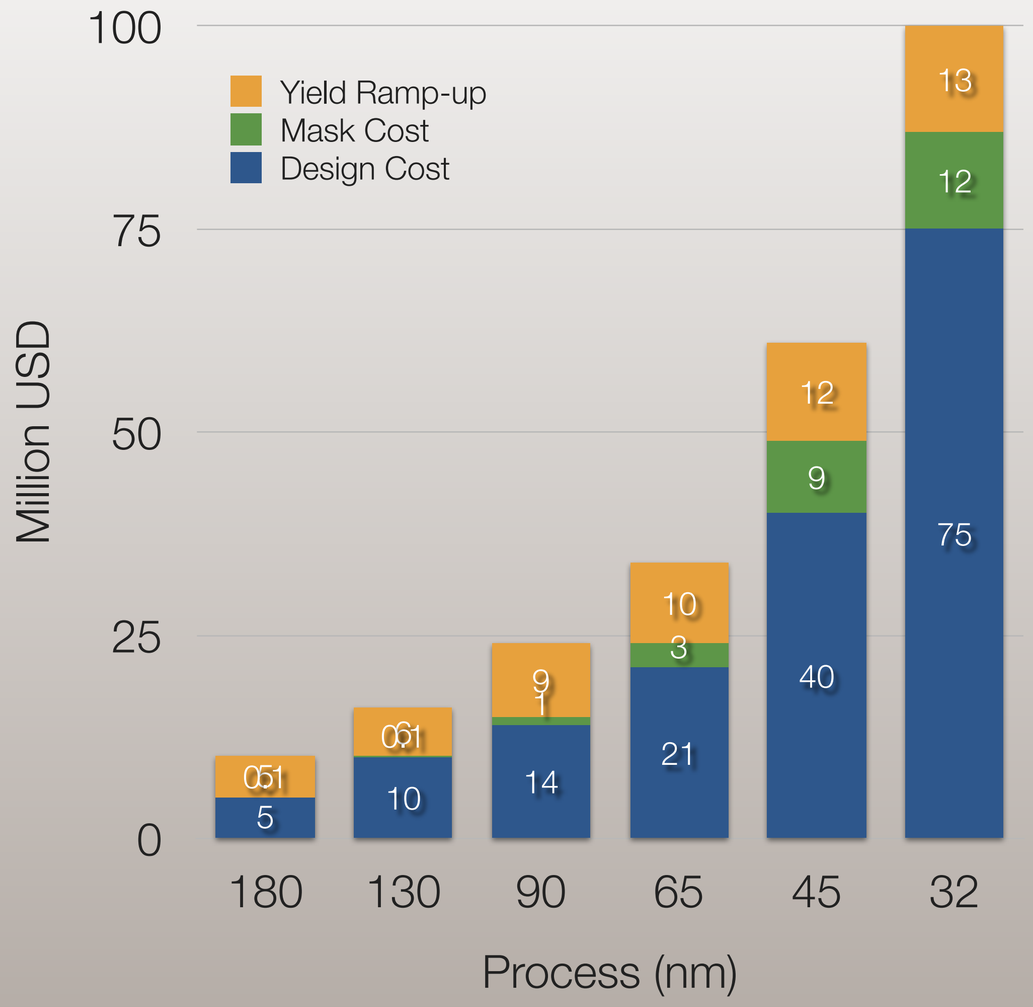
- Logic design → Place & route, then you'll get a chip
- Steady effort in process technologies (in lithography)
  - x2 density in 1.5 years: Moore's law
    - More density brings more feature
  - Smaller transistors are faster: higher performance without design effort

Reality is not

- Making things smaller is not easy
  - Smaller transistor has more leak currents: larger power consumption
  - Thinner wire has more parasitic capacitance: slower signal propagation
- Lithography costs are skyrocketing
  - Already impossible with visible lights, EUV (Extreme Ultraviolet) is still hard

LSI design costs

* State-of-the-art process has…
  * More cost for design and masks
  * Available for only limited products

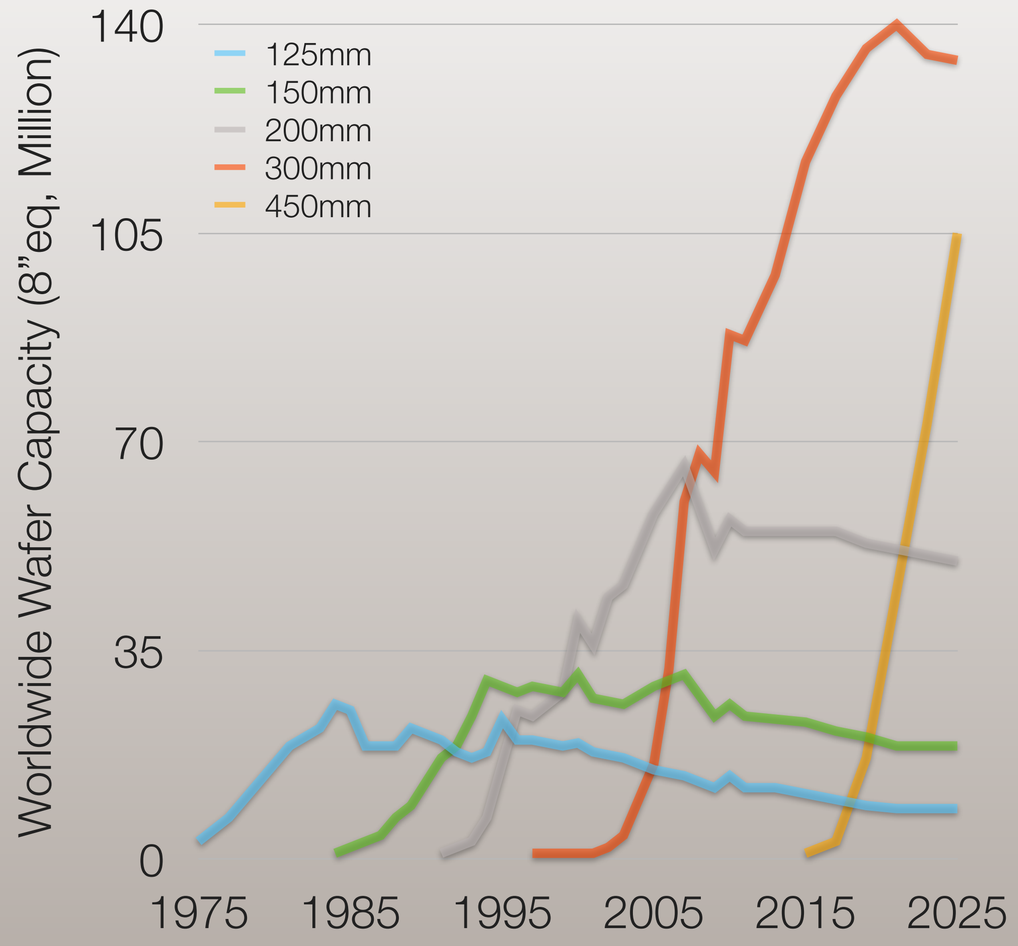


IC design costs at different process nodes

Ilkka Tuomi, “The Future of Semiconductor Intellectual Property Architectural Blocks in Europe”, JRC European Commission, 2009

Trends in wafer size

- Larger wafer brings cheaper chip
  - Requires enough product volume
- For small dies, smaller wafer is still enough
  - Thus 125mm and 150mm are still active



450 mm Era: A New Opportunity for the Semiconductor Industry

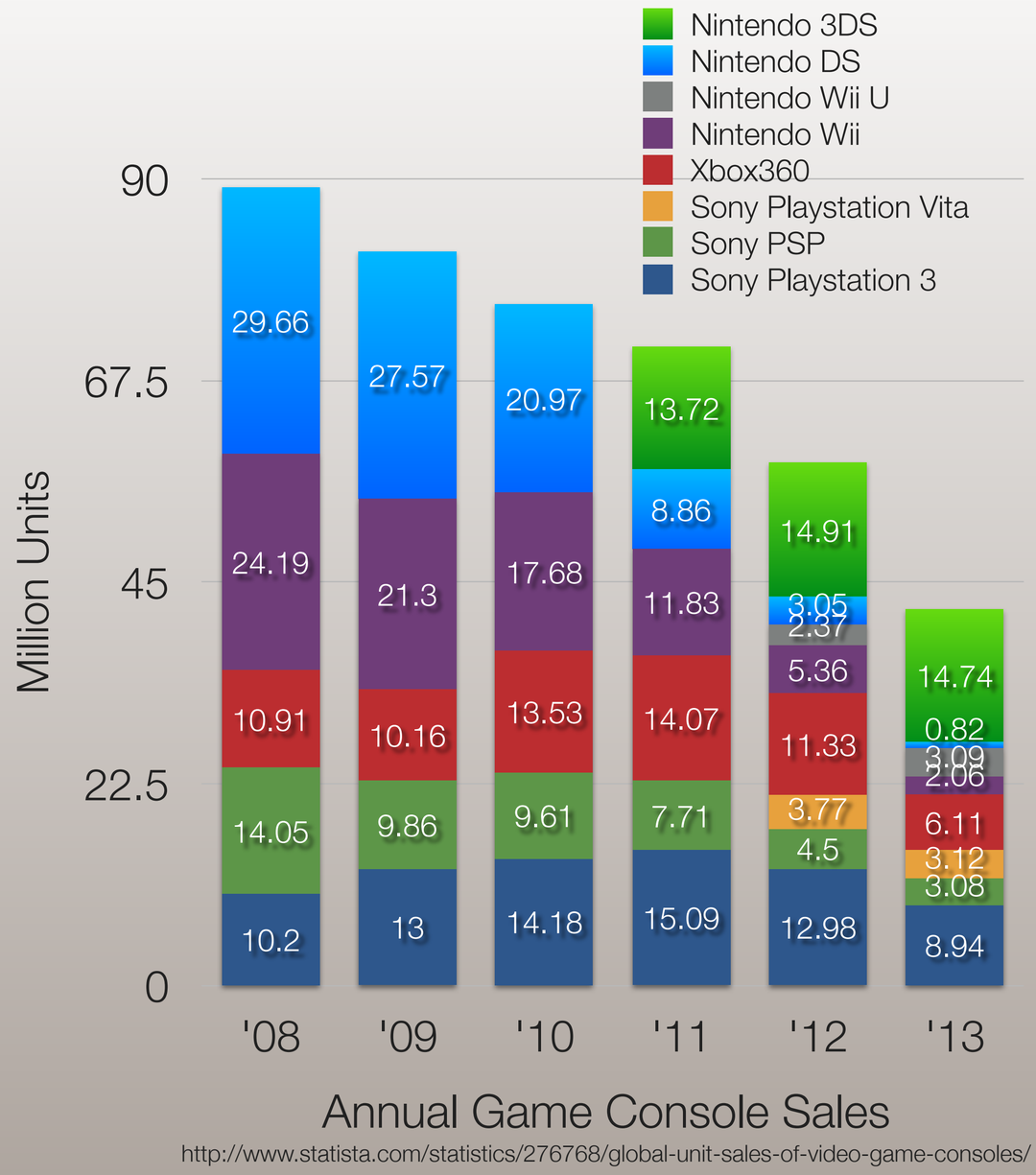
(4/25/2013) Future Fab Intl. Issue 45

LSI prototyping

- Demand of “Prototyping” an LSI
  - Circuit simulation on computers are not perfect, not very fast
  - Can’t completely test interactions with other devices on the board
- Prototyping with FPGA is an important step
  - For small product volume, shipment with FPGAs is a realistic option

Game consoles

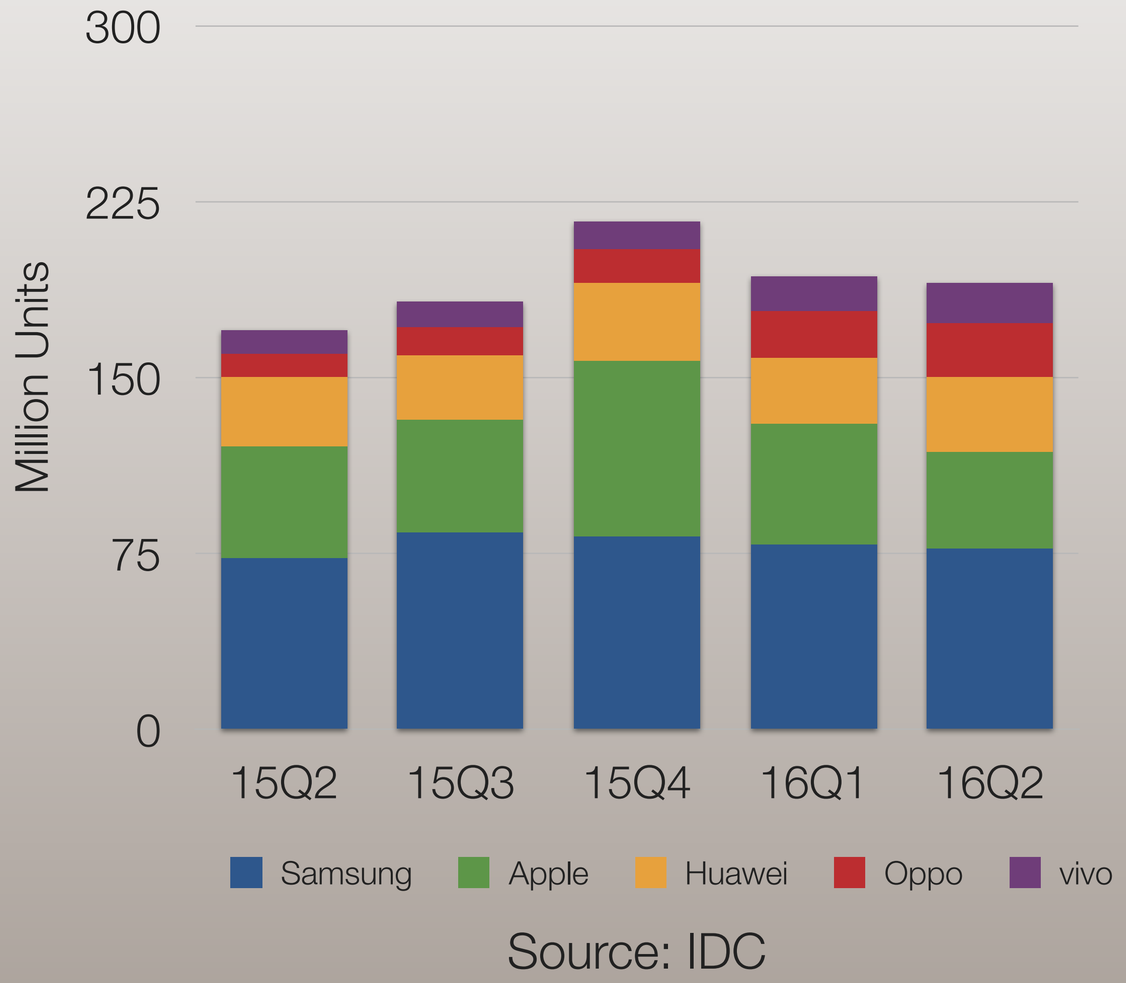
- Custom LSI with powerful CPU and GPU
  - XBox360: IBM PowerPC (90, 65nm)
  - Playstation 3: Cell BE (90, 65, 45nm)
- Others are MIPS / ARM based SoC



http://www.statista.com/statistics/276768/global-unit-sales-of-video-game-consoles/

Global Smartphone sales

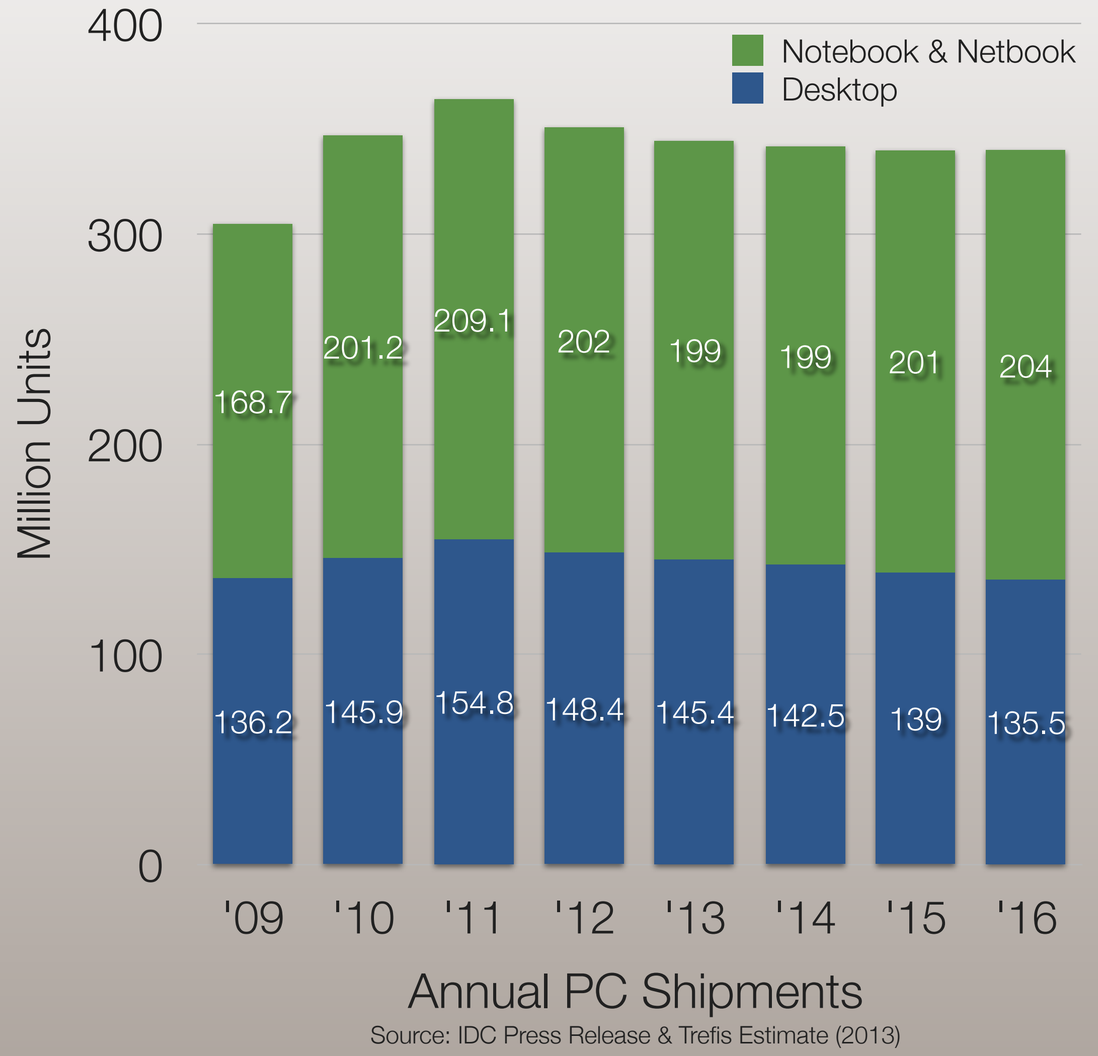
* Top 5 vendors
  * Custom SoCs: Samsung, Apple and Huawei
  * SoC suppliers: Qualcomm and MediaTek for other vendors
  * Mostly based on ARM processor



Source: IDC

Global PC sales

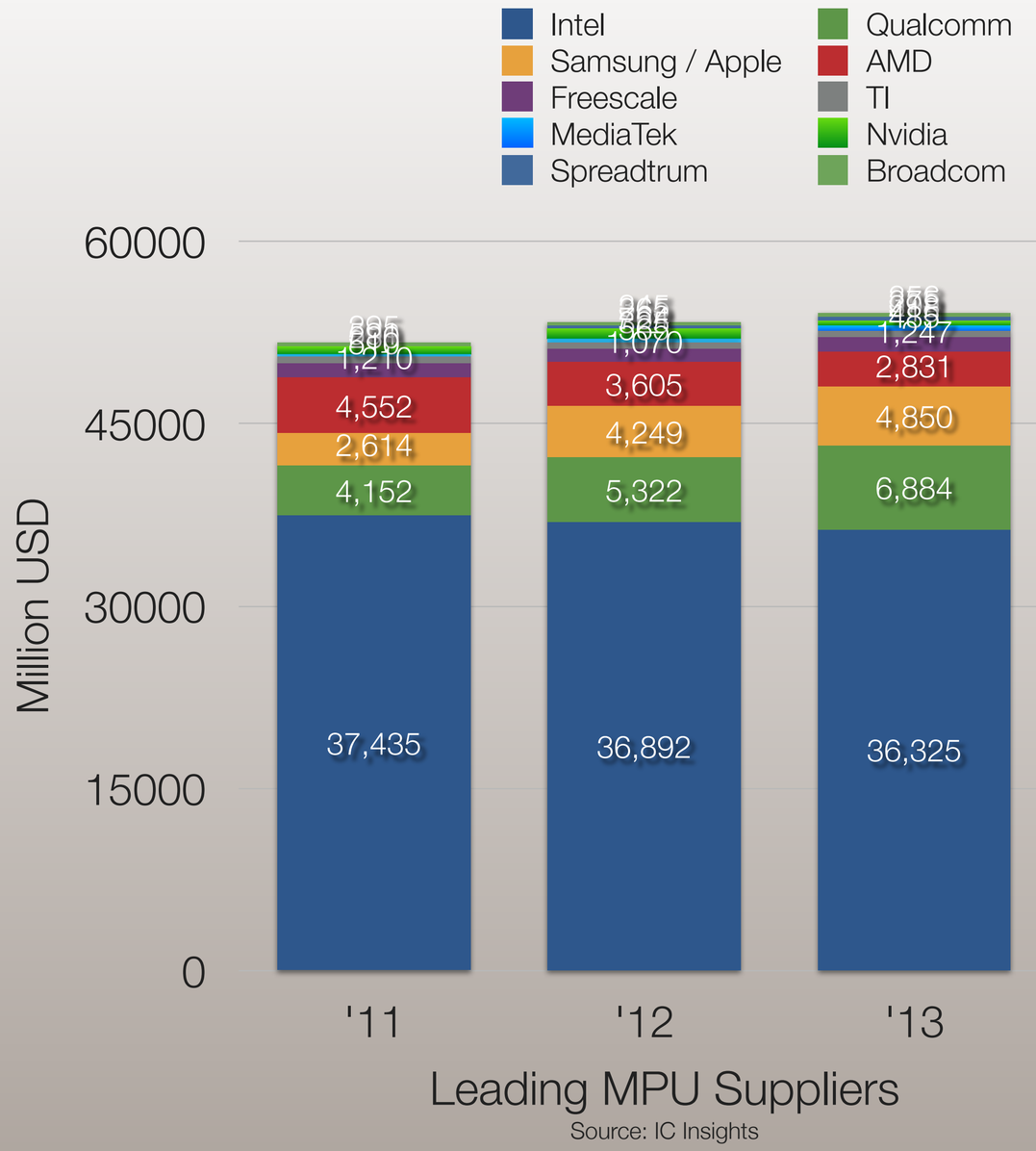
* CPUs for PC is one of most expensive LSI
  * Technology driver for logic LSI
  * Intel reached 14nm (Broadwell / Skylake)



Source: IDC Press Release & Trefis Estimate (2013)

MPU (CPU) Sales

* $30B drives the leading-edge process

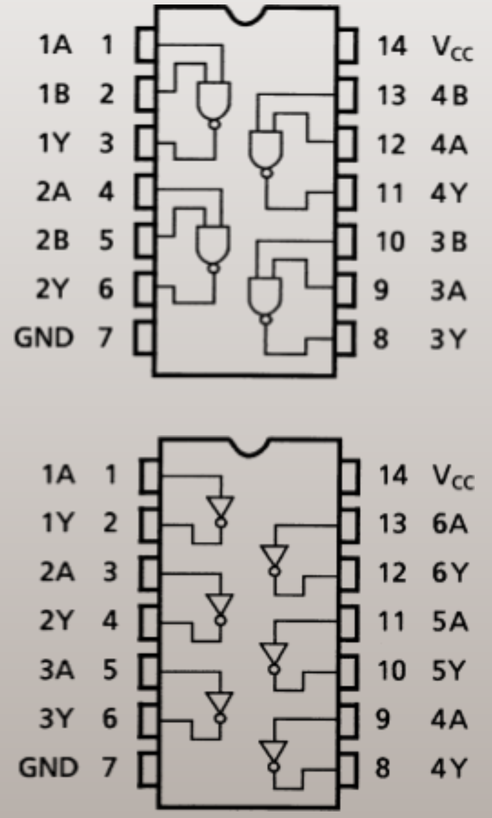


Reconfigurable devices

- Can “Program” logic circuits after production
  - Manufacture as a “standard” component
  - Use as “specialized” component in product
- One-time programmable / In-system programmable

Discrete logic ICs

- 74 series, 54 series, 40xx series …
  - ICs come with several logic gates
  - Building blocks for custom logic circuits
- Limited speed and requires larger circuit board



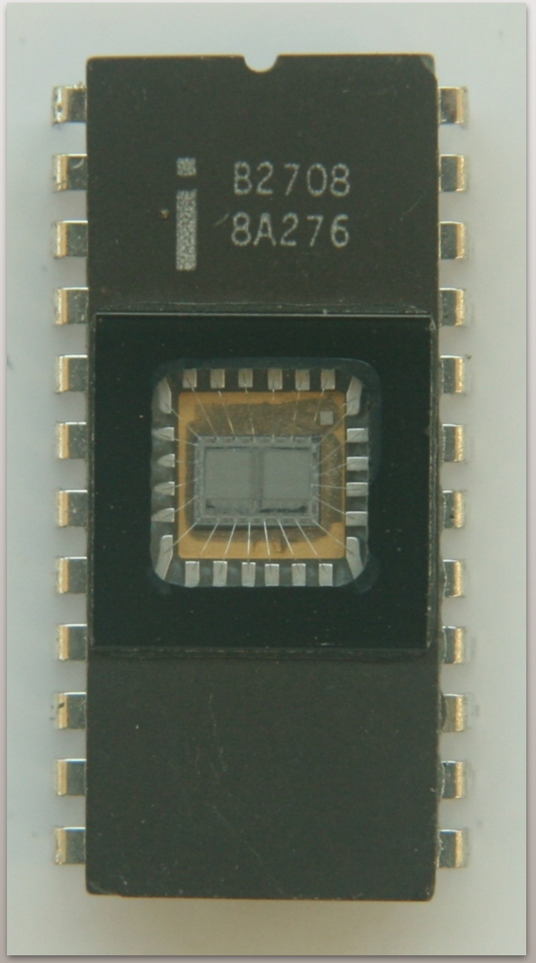
Source: Toshiba TC74HC00/04 datasheets

Glue Logic

- Miscellaneous logic between LSIs
  - Something like “part for glueing”
  - Always required in digital design, discrete logic ICs were there
    - Demands for “smaller, faster and cheaper”

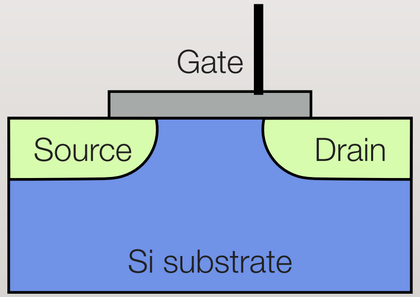
Programmable?

* Memory is programmable
  * Definitely, RAM is
  * Also, UVEPROMs and EEPROMs are
* Input (address) → Output (data)
  * or, any logic function

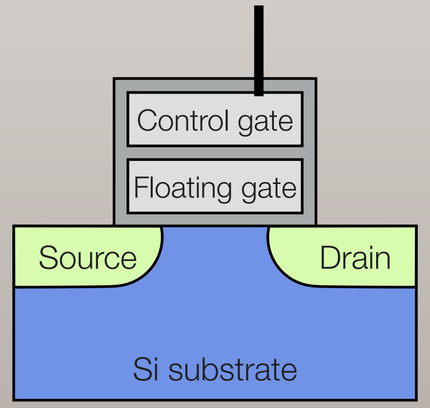


Floating gate MOS-FET

* Normal MOS-FET gate has only oxidized Si
* EEPROM has control / floating gates inside
  * High voltage on control gate to “inject” charge in floating gate. On substrate to “eject”.
* Charges in floating gate never goes outside



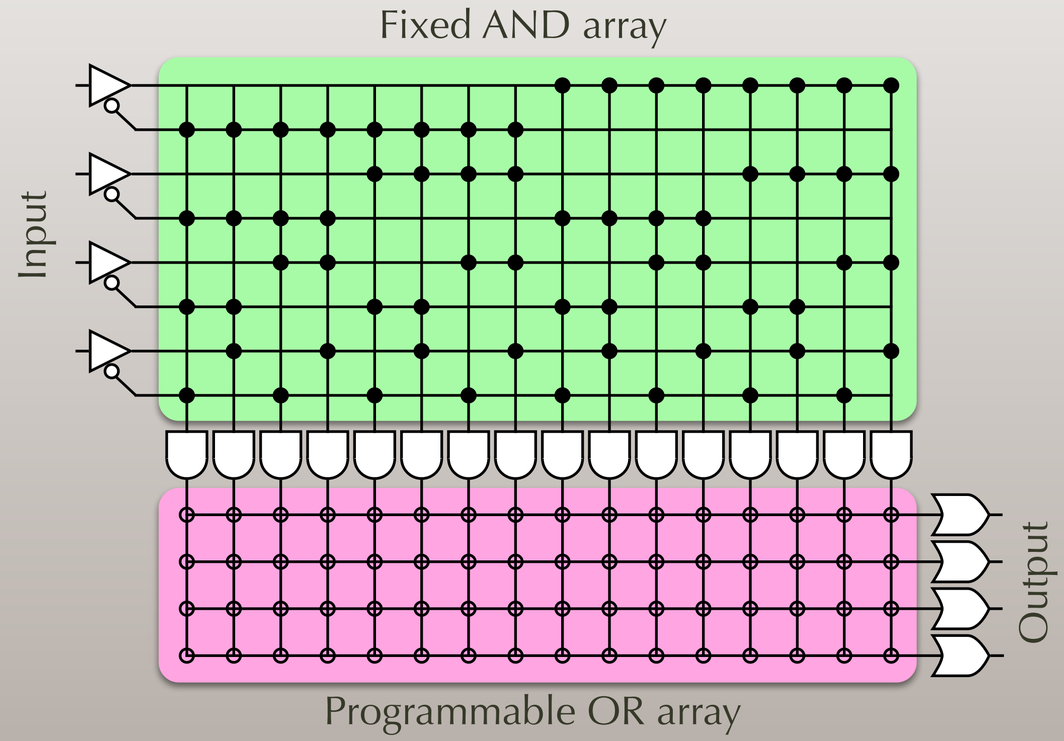
MOS-FET



EEPROM

Structure of PROMs

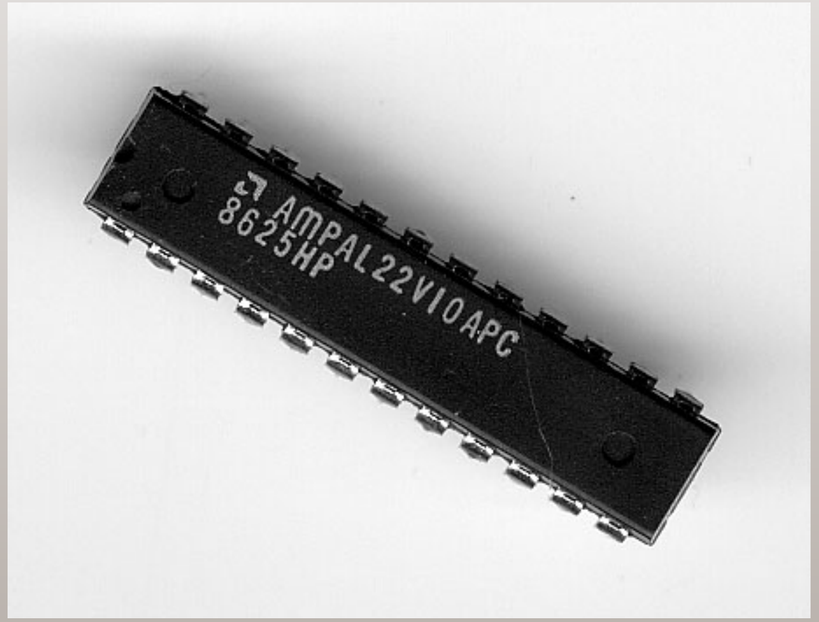
- Programmable ROM
  - Fixed address decoder (AND array)
  - Variable OR array to hold data
    - Fully-programmable output



* AND/OR symbols are PLD notation

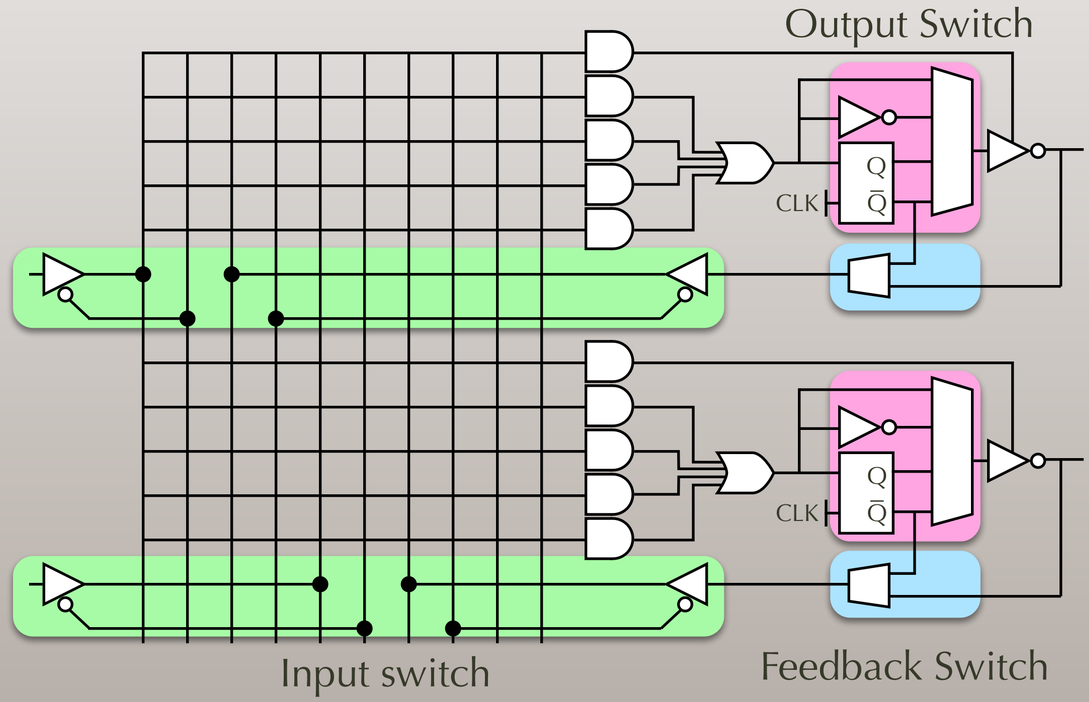
PAL, PLA: Programmable Array Logic

- PROM has fixed AND array + variable OR
  - PAL: variable AND + fixed OR
  - PLA: variable AND + variable OR
- “22V10” means 12-input + 10-output



GAL: Generic Array Logic

- PAL, PLA provides only sequential logic
  - GAL has FF + feedbacks to build sequential logic
  - Mostly same logic density as PALs and PLAs, such as GAL22V10

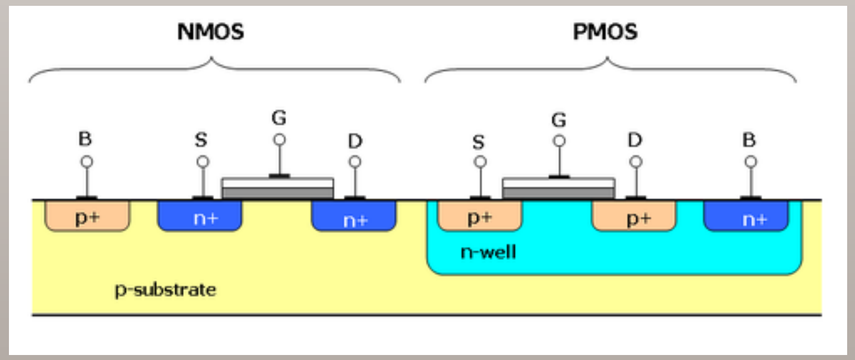


Device technologies

- Reconfigurability is provided by:
  - SRAM: flip-flops
  - EEPROM: floating gate MOS-FETs
  - Antifuses

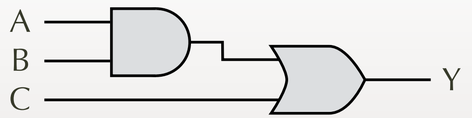
What is “Reconfigurable”

- Everything are on CMOS LSI: Transistors and wires are fixed
- But we can program:
  - Logics on the chip
  - Wirings on the chip (through switches)
  - I/O voltages

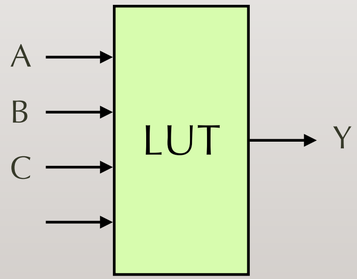


http://en.wikipedia.org/wiki/CMOS

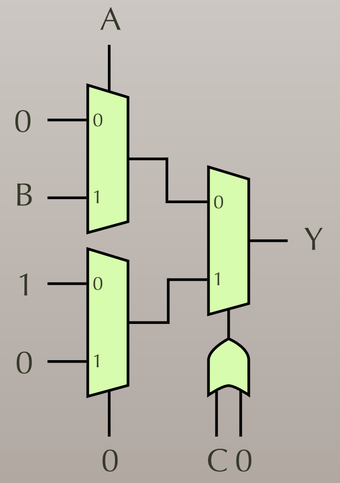
Logic cells



- Provides “any” logic functions
  - Memories (LUT: look-up table)
    - Simply remembers the truth table
  - Multiplexers
    - Programmed by “Select” signals



A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

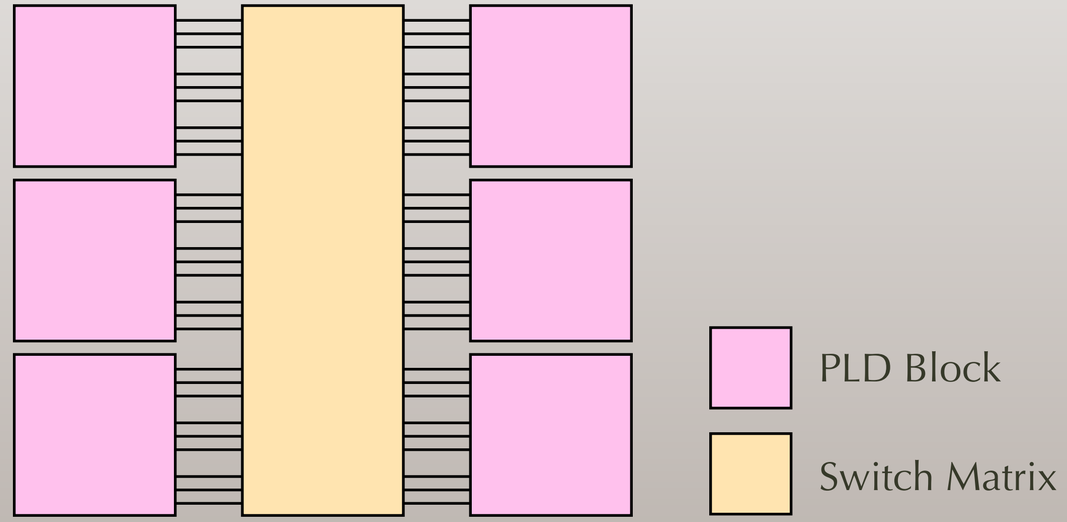


Classes of reconfigurable devices

* CPLD: Complex PLDs
* FPGA: Field-programmable Gate Arrays
* Coarse-grain

CPLD: Complex PLDs

- Multiple PLDs (PALs, GALs) on a chip
  - PLD blocks with switch matrix
    - Not actively used in these days
  - Nonvolatile as PLDs are

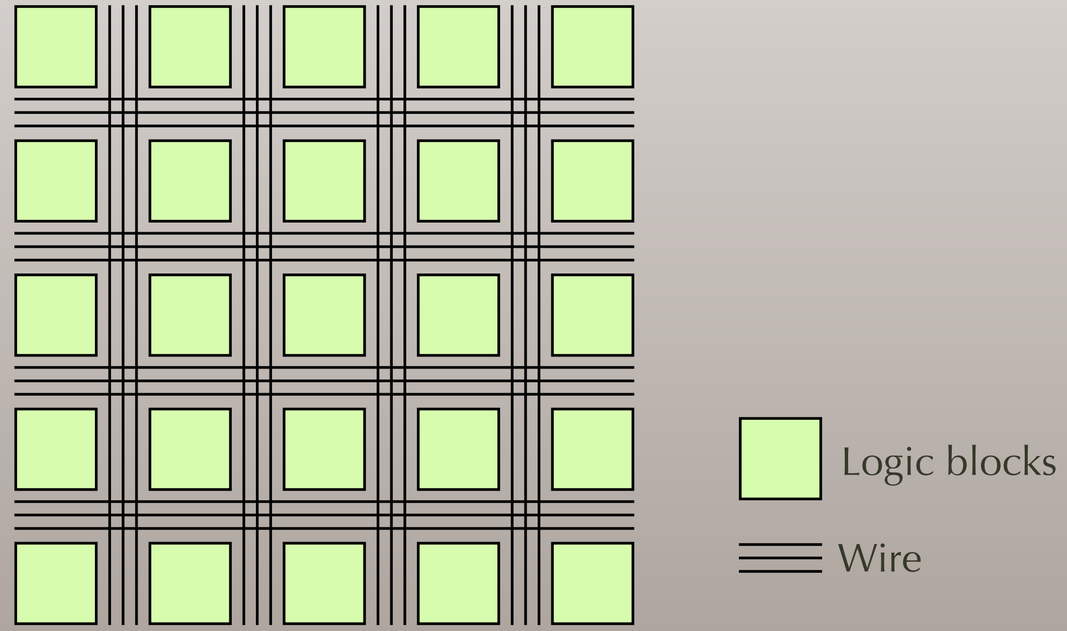


Gate arrays (not about FPGAs)

- Also called as ULA: uncommitted logic array
  - “Ready-made” Logic gates are already constructed on wafers
    - Users design their own metal wiring layers
  - Relatively cheaper and requires shorter design time for semi-custom LSIs

FPGA: Field Programmable Gate Array

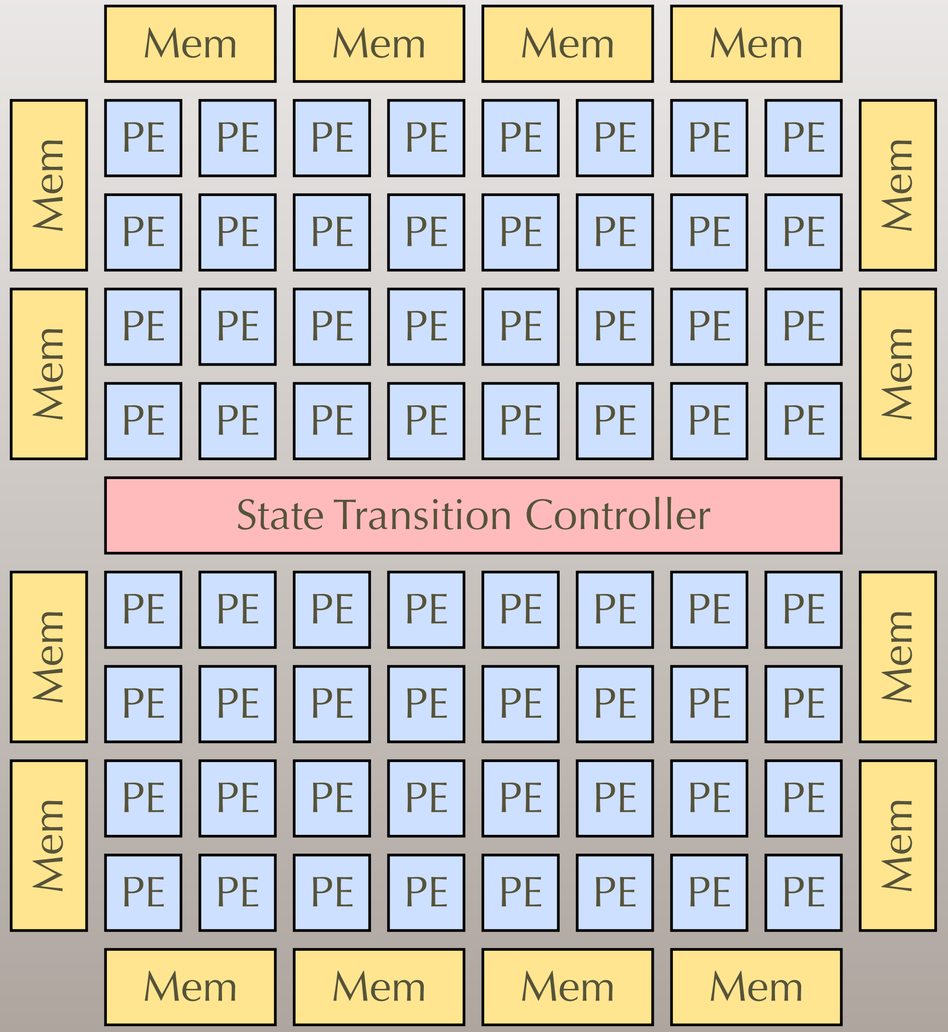
- Regularly arranged logic blocks and interconnects
  - Logic blocks are basically LUTs
    - 4-LUTs were popular
  - Highly flexible interconnects
- Island-style is popular

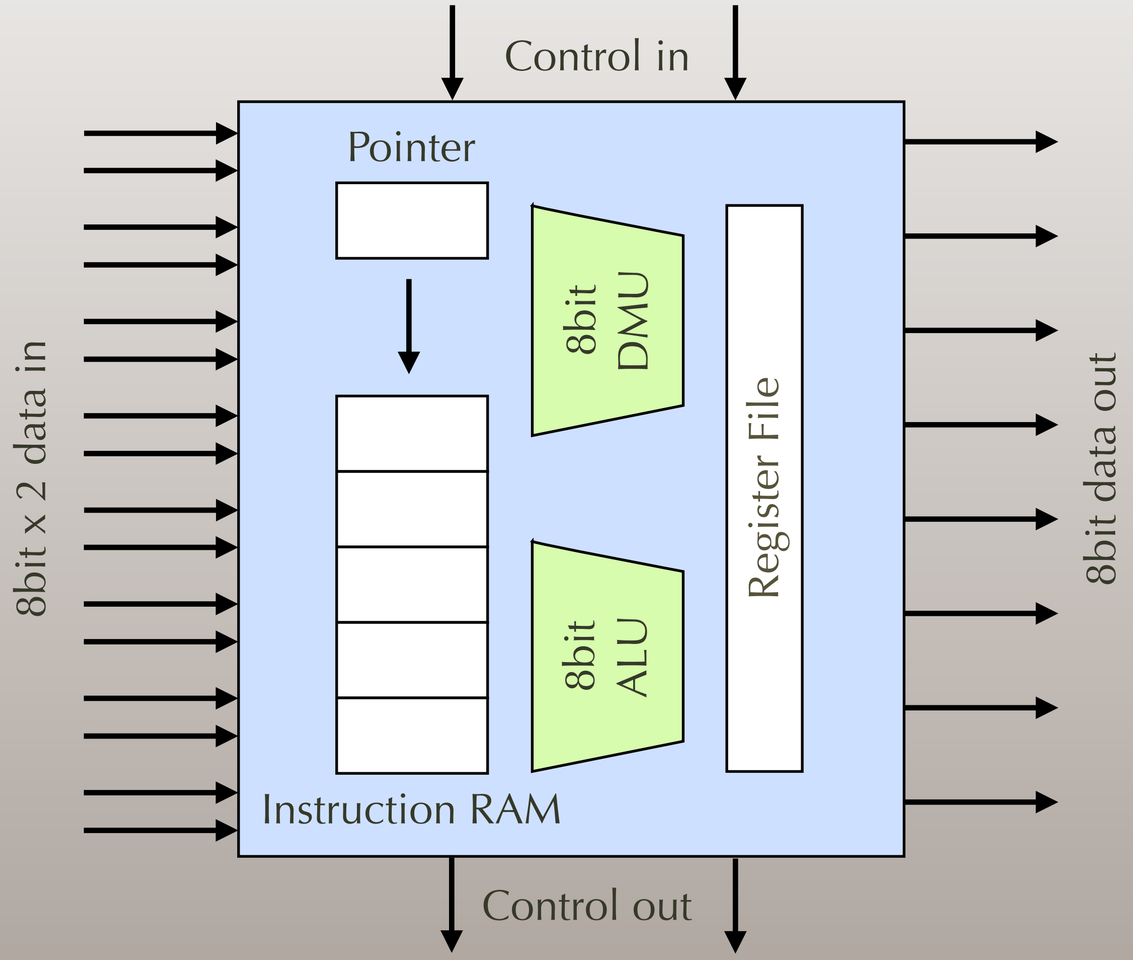


Coarse-grained devices

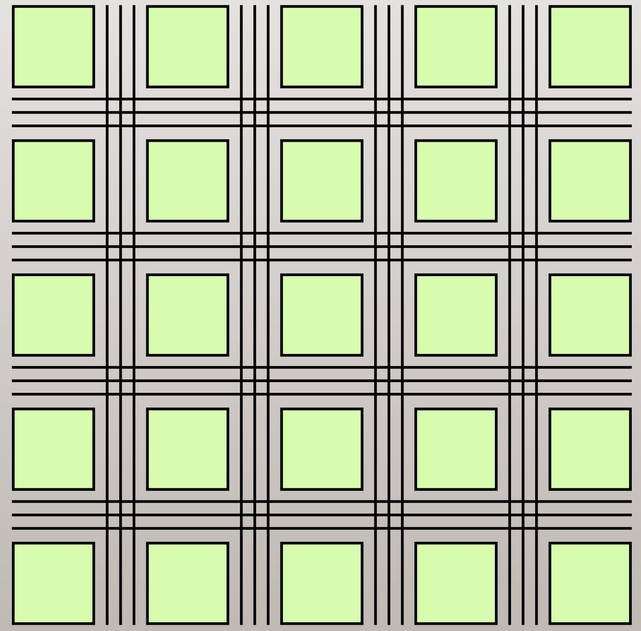
- PLDs and FPGAs are “Logic” device (i.e., not a “computing” device)
  - Any logic circuit can be implemented on
  - Also called “fine-grained” reconfigurable devices
- Coarse-grained devices has many arithmetic units
  - Suitable for signal processing or computing, not for logic.

NEC DRP (Renesas STP Engine)

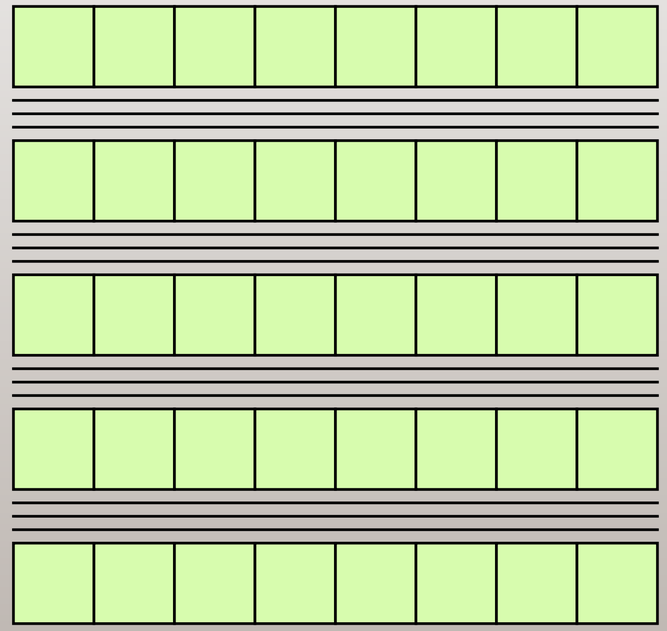




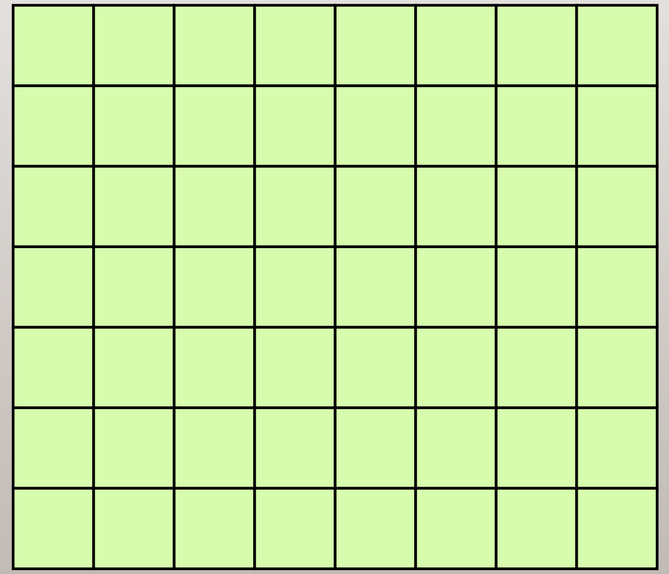
Device organization



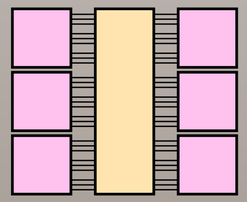
Island-style



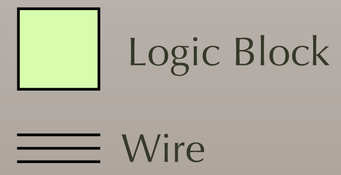
Channel-style



Sea-of-gate style



Please remember CPLD style….



Summary

- LSI design cost
  - Moore’s law is slowing down
  - Especially in edge process
  - High-mix low-volume is difficult
  - ~~Custom chip for every product~~
- Reconfigurable device is the key
  - PROMs, PLDs then FPGAs
  - Coarse-grain devices is fading out (but they may return)

Setup for your design environment

- FPGA boards
  - Digilent Nexys 4, Nexys 4 DDR, or Nexys A7 board
  - You can borrow one, please return by March
- CAD: Vivado HLx Design Suite **2018.2** (Webpack edition)
  - Install your PC for your design

CAD: Vivado HLx Design Suite (1)

- Ubuntu 16.04, 18.04 or Windows 8.1, 10.1
  - 64bit required
  - Larger RAM (4GB+) is preferred
  - Available from http://www.xilinx.com/support/download/
    - Registration required
- Older version for this class, because of SDK available with less disk usage

CAD: Vivado HLx Design Suite (2)

Productivity	Feature	WebPACK	Design Edition	System Edition
IP integration and debug	IDE	○	○	○
	SDK	○	○	○
	Partial reconfiguration	○	○	○
Verification and Debug	Simulator	○	○	○
	Logic Analyzer	○	○	○
	Serial I/O Analyzer	○	○	○
Design Exploration and IP generation	High-level synthesis	○	○	○
	System Generator for DSP			○

CAD: Vivado HLx Design Suite (3)

- Webpack: Free of costs, useful for personal development (but not limited to)
  - with limitation of target FPGAs
- Design Edition: Cheaper choice ($2,995-,1 year subscription)
- System Edition: Fully-featured ($4,795-, 1 year subscription)
  - If you need fully-featured version for you research, Xilinx-donated license is available within the dept. of EEE (ask me.)

CAD: Vivado HLx Design Suite (4)

* Just ignore for license setup for webpack edition.